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| EXAMINER | |
|---|---|
| LEVITAN, DMITRY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2662 | |

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/630,413 | DEMAKAKOS ET AL. | |
| | Examiner | Art Unit | |
| | Dmitry Levitan | 2662 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19,21-33,35-40,42-44 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19, 21-33, 35-40, 42-44 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Amendment, filed 10/12/05 has been entered. Claims 1-19, 21-33, 35-40, 42-44 and 46 remain pending.

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 36-40 and 42-46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36 recites the limitation "the first and second selectably-activated loopback circuits" in line 18. There is insufficient antecedent basis for this limitation in the claim.

Claim 43 recites the limitation "the first and second selectably-activated loopback circuits" in line 23. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 103*

1. Claims 1-3, 7-9, 11-14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton (US 5,343,461) in view of Gewin (US 5,060,226).

2. Regarding claim 1, Barton substantially teaches the limitations of claims 1:

A first input port (REV port of path 12 on Fig. 2 and 3, 16:60-67 and 17:1) for connection to a first digital carrier link for coupling to a digital network (DS1 facility 15 on Fig. 1-3);

A first output port (RCV OUT port of path 12 on Fig. 2 and 3) for connection to a second digital carrier link for coupling to a digital terminal equipment (CPE 20 on Fig. 2 and 3);

A first path between the first input and output ports (path 12 on Fig. 2);

A second input port (XMT IN port of path 14 on Fig. 2 and 3) for connection to the second digital carrier link for coupling to a digital terminal equipment;

A second output port (XNT OUT port of path 14 on Fig. 2 and 3) for connection to the first digital carrier link for coupling to a digital network;

A second path between the second input and output ports (path 14 on Fig. 2);

A first selectively-activated loopback circuit (using loop-up or loop down codes 17:18-25) which when activated provides a third path between (using K1 relays on Fig. 2 and 3, 18:7-19) the first input port and the second output port;

A controller coupled to the first selectively-activated loopback circuit (loopback code detector on Fig. 2 and 3, 18:7-19) to activate it individually.

Barton does not teach a second selectively activated loopback circuit, a controller to activate the second loopback circuit and controller to activate the first and second loopbacks simultaneously.

Gewin teaches a second selectively activated loopback circuit (far and near side loopbacks as shown on Fig. 1B and 2:25-35) and a controller to activate the second loopback circuit (detector 46, synchronizer 50, reset comparator 48, comparator 56, timer 54, timing and control 60 and data selector 58 on Fig. 1B monitoring the near and far sides 6:7-15) and activating the first and second loopbacks simultaneously (activating relay 64 on Fig. 1B and 6:54-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a second loopback, its circuit activation and simultaneous activation of

both loopbacks in the controller of Gewin into the system of Barton to improve the system loopback capabilities for near and far sides.

Regarding claim 2, Barton teaches the first signal path comprising a first signal regenerator and the second signal path comprising a second signal regenerator (regenerators 24 connected to paths 12 and 24, as shown on Fig. 2 and 15:48-62).

Regarding claim 3, Barton teaches a multi-position switch to activate the first regenerator in first position and de-activate in a second (switch 143 on Fig. 6 and 31:12-27).

Regarding claims 7 and 8, Barton teaches a line build-out circuit and pre-equalizing build-out circuit(automatic line build-out 34 on Fig. 2 and 17:8-10 and 18:56-59).

Regarding claim 9, Barton teaches a selectably-enabled power supply to provide power to the second carrier link (DC CON on Fig. 6 and 35:25-45).

Regarding claim 11, Gewin teaches the controller comprises a first/second loopback code detector (date selector 58 on Fig. 1B, monitoring first and second inputs 62 and 72 6:8:15) configured to:

If the first/second loopback circuit is de-activated, detect a loopback code received at the related input port and activate the first/second loopback circuit (activating normally dormant/transparent units 1:20-23 with a loop back code to activate both first and second loopbacks as on Fig. 1B and 6:45-67); and

Detect loop-down code received at the first/second input port and then de-activate both first and second loopback circuits, if in an active state (detecting reset code to terminate both loopbacks, Fig. 1B and 7:3-16).

Regarding claims 12-14, Barton teaches four jacks (Fig. 3), two for non-intrusive monitoring/signal detection (RCV BRG and XMT BRG) and two for signal access/injection (EQ IN on network side and EQ OUT on terminal side).

Regarding claims 17 and 18, Barton teaches input and output ports connected to transmission span 10 on Fig. 1 disclosed as DS1 or T1 facility 15:36-46).

3. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton and Gewin in view of Admitted Prior Art disclosed in the specification on page 14 lines 11-16 and Bergstrom (US 5,521,977).

Barton and Gewin substantially teach the limitations of claims 15 and 16.

Barton and Gewin do not teach format detectors coupled with visual indicators identifying types of frame formats.

Admitted prior art teaches first and second format detectors to determine first and second formats of signals on first and second paths are one of unframed, SF/D4 and T1-ESF.

Bergstrom teaches a visual indicator (LED) that flashes when the system is in timed loopback (11:49-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add three indicators of Admitted Prior Art identifying three types of loop backs as LED of Bergstrom, making them visual, to the system of Barton and Gewin to improve the system visual loop back presentation.

4. Claims 4, 22-26, 29, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton (US 5,343,461) in view of Gewin (US 5,060,226) and Garcia (US 5,224,149).

5. Regarding claims 4, 22 and 36, Barton substantially teaches the limitations of claims 4, 22 and 36:

A first input port (REV port of path 12 on Fig. 2 and 3, 16:60-67 and 17:1) for connection to a first digital carrier link for coupling to a digital network (DS1 facility 15 on Fig. 1-3);

A first output port (RCV OUT port of path 12 on Fig. 2 and 3) for connection to a second digital carrier link for coupling to a digital terminal equipment (CPE 20 on Fig. 2 and 3);

A first path between the first input and output ports (path 12 on Fig. 2);

A second input port (XMT IN port of path 14 on Fig. 2 and 3) for connection to the second digital carrier link for coupling to a digital terminal equipment;

A second output port (XNT OUT port of path 14 on Fig. 2 and 3) for connection to the first digital carrier link for coupling to a digital network;

A second path between the second input and output ports (path 14 on Fig. 2);

A first signal regenerator coupled between the first input and output (regenerator 24 on Fig. 2 and 3, 15:57-63);

A first selectively-activated loopback circuit (using loop-up or loop down codes 17:18-25) which when activated provides a third path between (using K1 relays on Fig. 2 and 3, 18:7-19) the first input port and the second output port;

A controller coupled to the first selectively-activated loopback circuit (loopback code detector on Fig. 2 and 3, 18:7-19) to activate it individually.

Barton does not teach a second loopback and a controller to activate it, and to activate the first and second loopbacks simultaneously and a second signal regenerator coupled between second input and output.

Gewin teaches a second loopback circuit (far and near side loopbacks as shown on Fig. 1B and 2:25-35), a controller to activate the second loopback circuit (detector 46, synchronizer 50, reset comparator 48, comparator 56, timer 54, timing and control 60 and data selector 58 on Fig. 1B monitoring the near and far sides 6:7-15) and activate the first and second loopbacks simultaneously (activating relay 64 on Fig. 1B and 6:54-63).

Garcia teaches a second signal regenerator coupled between second input and output (regenerator 64 on Fig. 1 and 2, 4:37-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate second loopback circuit and simultaneous activation of both loopbacks in the controller of Gewin and a second regenerator of Garcia into the system of Barton to improve the system loopback capabilities for near and far sides.

In addition, regarding claim 36, Barton teaches first and second monitoring jacks for non-intrusively monitoring the first and second paths (RCV BRIDG and jack 181 on Fig. 3 and 6, 31:61-67 and 32:1).

Regarding claims 23 and 25, Gewin teaches the controller comprises a first/second loopback code detector (date selector 58 on Fig. 1B, monitoring first and second inputs 62 and 72 6:8:15) configured to:

If the first/second loopback circuit is de-activated, detect a loopback code received at the related input port and activate the first/second loopback circuit (activating normally

dormant/transparent units 1:20-23 with a loop back code to activate both first and second loopbacks as on Fig. 1B and 6:45-67); and

Detect loop-down code received at the first/second input port and then de-activate both first and second loopback circuits, if in an active state (detecting reset code on any of the first or second inputs to terminate both loopbacks, Fig. 1B and 7:3-16).

Regarding claims 24 and 26, Gewin teaches first/second loopback detector is adapted to detect loop-up and loop-down codes in a plurality of formats (using codes of any sufficient length N as loop-up and loop-down codes 9:23-27).

Regarding claim 29, Barton teaches four jacks (Fig. 3), two for non-intrusive monitoring/signal detection (RCV BRG and XMT BRG) and two for signal access/injection (EQ IN on network side and EQ OUT on terminal side).

Regarding claim 32, Barton teaches input and output ports connected to transmission span 10 on Fig. 1 disclosed as DS1 or T1 facility 15:36-46).

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barton (US 5,343,461) in view of Gewin (US 5,060,226) and Garcia (US 5,224,149).
Regarding claim 28, Barton, Gewin and Garcia substantially teaches the limitations of claim 28, including a pre-equalized circuit for the first regenerator, but they do not teach a pre-equalized circuit to shape the second regenerated signal before it reaches the second output port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate second pre-equalizer to shape the signal for the second generator into the system of Gewin, Garcia and Barton, if needed, to correct signal level for the DSX1/T1 loop.

7. Claims 30, 31 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton (US 5,343,461), Gewin (US 5,060,226) and Garcia (US 5,224,149) in view of admitted prior art disclosed in the specification on page 14 lines 11-16 in further view of Bergstrom (US 5,521,977).

Barton substantially teaches the limitations of claims 30, 31 and 37-39.

Barton does not teach first and second format detectors to determine first and second formats of signals on first and second paths and first and second indicators to provide first and second plurality of visual indications based on first and second formats.

Admitted prior art teaches first and second format detectors to determine first and second formats of signals on first and second paths on first and second paths are one of unframed, SF/D4 and T1-ESF.

Bergstrom teaches a visual indicator (LED) that flashes when the system is in timed loopback (11:49-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate first and second format detectors of Admitted Prior Art to determine first and second formats of signals on first and second paths and first and second indicators to display the formats into system of Barton to improve visual indication of the signals received by the system.

8. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton, Gewin and Garcia in further view of Bergstrom (US 5,521,977).

Barton, Gewin and Garcia substantially teach the limitations of claims 5 and 6.

Barton, Gewin and Garcia do not teach three visual indicators identifying three types of loop backs.

Bergstrom teaches a visual indicator (LED) that flashes when the system is in timed loopback (11:49-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was to use visual indicators of Bergstrom three times identifying three types of loop backs to the system of Barton, Gewin and Garcia to improve the system visual loop back presentation.

9. Claims 10 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton, Gewin and Garcia in further view of Jenkins (US 4,107,469).

Barton, Gewin and Garcia substantially teach the limitations of claims 10 and 27, including manual loop back switches on Fig. 6 and switches 203 and 205 37:6-19).

Barton, Gewin and Garcia do not teach three position switch to activate three types of loop backs.

Jenkins teaches using multi-position switch to combine several switch functions in one switch (Multi-position switch on Fig. 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to using multi-position switch of Jenkins to activate three types of loop backs to the system of Barton, Gewin and Garcia to combine three separate switches into one to save the system cost and space.

10. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barton (US 5,343,461) in view of admitted prior art disclosed in the specification on page 14 lines 11-16 in further view of Gewin and Bergstrom (US 5,521,977).

Barton substantially teaches the limitations of claim 43:

A first input port (REV port of path 12 on Fig. 2 and 3, 16:60-67 and 17:1) for connection to a first digital carrier link for coupling to a digital network (DS1 facility 15 on Fig. 1-3);

A first output port (RCV OUT port of path 12 on Fig. 2 and 3) for connection to a second digital carrier link for coupling to a digital terminal equipment (CPE 20 on Fig. 2 and 3);

A first path between the first input and output ports (path 12 on Fig. 2);

A second input port (XMT IN port of path 14 on Fig. 2 and 3) for connection to the second digital carrier link for coupling to a digital terminal equipment;

A second output port (XNT OUT port of path 14 on Fig. 2 and 3) for connection to the first digital carrier link for coupling to a digital network;

A second path between the second input and output ports (path 14 on Fig. 2);

First and second monitoring jacks for non-intrusively monitoring the first and second paths (RCV BRIDG and jack 181 on Fig. 3 and 6, 31:61-67 and 32:1);

Visual indicator (loss of signal LED 25:34-39),

A controller coupled to first selectively-activated loopback circuit (loopback code detector on Fig. 2 and 3, 18:7-19) to activate it individually.

Barton does not teach first and second format detectors to determine first and second formats of signals on first and second paths and first and second indicators to provide first and second plurality of visual indications based on first and second formats, a second selectively

activated loopback circuit, a controller to activate the second loopback circuit and controller to activate the first and second loopbacks simultaneously.

Admitted prior art teaches first and second format detectors to determine first and second formats of signals on first and second paths.

Bergstrom teaches a visual indicator (LED) that flashes when the system is in timed loopback (11:49-50).

Gewin teaches a second selectively activated loopback circuit (far and near side loopbacks as shown on Fig. 1B and 2:25-35) and a controller to activate the second loopback circuit (detector 46, synchronizer 50, reset comparator 48, comparator 56, timer 54, timing and control 60 and data selector 58 on Fig. 1B monitoring the near and far sides 6:7-15) and activating the first and second loopbacks simultaneously (activating relay 64 on Fig. 1B and 6:54-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate first and second format detectors of Admitted Prior Art to determine first and second formats of signals on first and second paths and first and second indicators to display the formats into system of Barton to improve visual indication of the signals received by the system and to incorporate second loopback, its circuit activation and simultaneous activation of both loopbacks in the controller of Gewin into the system of Barton to improve the system loopback capabilities for near and far sides.

11. Claims 19, 21, 33, 35, 40, 42, 44 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barton, Gewin and Garcia and in further view of Admitted Prior art (page 9, lines 11-19).

Barton, Gewin, Garcia substantially teach the limitations of claims 19, 33, 40 and 44.

Barton, Gewin, Garcia do not teach implementing the repeater on 200 or 400 type circuit cards.

Admitted Prior Art teaches implementing the repeater on 200 or 400 type circuit cards (Type-400 NCTE 9:11-19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add implementing the repeater on 200 or 400 type circuit cards of Admitted Prior Art to the system of Barton, Gewin, Garcia to improve the system compatibility with existing shelves.

Regarding claims 21, 35, 42 and 46, Barton teaches implementing the repeater on the card with 56 pin-outs (using 56 pin connector 27:43-52).

***Response to Arguments***

12. Applicant's arguments filed 10/12/05 have been fully considered but they are not persuasive.

On pages 13-16 of the Response, Applicant argues that Barton in view of Gewin does not teach a controller to selectively activate the first and second selectably-activated loopback circuits individually and simultaneously.

Examiner respectfully disagrees.

Barton teaches a controller to activate the first selectably-activated loopback circuit individually (loopback code detector on Fig. 2 and 3, performing a loopback test 18:7-19).

Gewin teaches a second loopback circuit and a controller to activate the first and second loopback circuits simultaneously 6:54-63.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a controller of Barton to independently activate a second loopback of Gewin in the same manner as the first loopback and add simultaneous activation of the both loopbacks of Gewin to the system of Barton to improve the system loopback capabilities for near and far sides.

Applicant's arguments regarding the implementation of simultaneous activation of Gewin are irrelevant, because Examine did not base the rejection on this portion of Gewin teachings.

On page 16 of the Response, Applicant argues that Garcia does not teach a second selectably-activated loopback circuit which, when activated loops the second regenerated signal to the first output port.

Examiner respectfully disagrees.

Gewin, not Garcia teach a second loopback circuit which, when activated loops the second signal to the first output port (see Gewin Fig. 1B and 3:50-65). Garcia teaches regenerating the loopback signal.

Applicant's arguments regarding the implementation of a second signal regenerator of Garcia are irrelevant, because Examine did not base the rejection on this portion of Garcia teachings.

*Conclusion*

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dmitry Levitan whose telephone number is (571) 272-3093. The examiner can normally be reached on 8:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DL

Dmitry Levitan
Patent Examiner.
10/25/05

JOHN PEZZLO
PRIMARY EXAMINER